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| 10/550,326 | 01/09/2007 | Roger D. Chamberlain | 53047-57365 | 2088 |

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| EXAMINER | |
|---|---|
| TOLENTINO, RODERICK | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2439 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 12/23/2010 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPDOCKET@THOMPSONCOBURN.COM

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/550,326 | CHAMBERLAIN ET AL. | |
| | Examiner | Art Unit | |
| | Roderick Tolentino | 2439 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 October 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23 and 45-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23 and 45-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/23/2010, 12/11/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1 – 23 and 45 – 64 are pending.

### *Response to Arguments*

2. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection, as necessitated by amendment by applicant on 10/27/2010.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 – 11, 13 – 23, 45 – 47, 51 – 53, 57 – 59, 63 and 64 are rejected under 35 U.S.C. 102(e) as being anticipated by Evoy U.S. PG-Publication No. (2006/0059213).

5. As per claims 1, 9, 20 and 53, Evoy discloses providing a reconfigurable logic device for bridging data transfers between a processor that requests the data transfers and the data store (Evoy, Paragraph 0066, FPGA used with access control

functionality), the reconfigurable programmable logic device receiving a stream of encrypted data from the data store (Evoy, Paragraph 0023, receive encrypted data stream), the reconfigurable logic device decrypting the received encrypted data stream to create decrypted data the reconfigurable logic device (Evoy, Paragraph 0023, decrypts encrypted stream), encrypting the decrypted data in a second encrypted format (Evoy, Paragraph 0023, re-encrypts a digital data stream that has been decrypted and Paragraph 0043, encryption designed to support any encryption/decryption algorithm) and sharing the data of the second encrypted format by communicating it to an authorized party wherein the decrypted data is not accessible to the processor (Evoy, Paragraph 0023, communicates re-encrypted digital stream over a channel which is not the processor and Paragraph 0010 content viewable by authorized users).

6. As per claim 2, Evoy discloses providing the authorized party with a key to decrypt the shared data (Evoy, Paragraph 0044, public key for decryption).

7. As per claims 3 and 10, Evoy discloses the second encrypted format is different than the first encrypted format such that the key provided to the authorized party will be different than a key necessary to decrypt the stored data (Evoy, Paragraph 0044, public key for decryption and Paragraph 0043, encryption designed to support any encryption/decryption algorithm).

8. As per claim 4, Evoy discloses providing a memory device in communication with the reconfigurable logic device, wherein the content of the memory device is accessible only by the programmable logic device, and wherein the reconfigurable logic device is

further configured to store at least a portion of the decrypted data in the memory device (Evoy, Paragraph 0056, circuitry coupled to a memory).

9. As per claims 5 and 22, Evoy discloses the data store is owned by a first party, and wherein the data stored in the data store is owned by a second party (Evoy, Paragraph 0042, data moves from memory to memory of the virtual channel).

10. As per claims 6 and 23, Evoy discloses receiving a request for stored data from the authorized party; responsive to the received request, retrieving stored data from the data store and processing the retrieved store4 data through the reconfigurable logic device to perform the decrypting and encrypting steps (Evoy, Paragraph 0023, receive encrypted data and decrypt encrypted data).

11. As per claim 7, Evoy discloses storing data in the data store in the first encrypted format (Evoy, Paragraph 0023, re-encrypts a digital data stream that has been decrypted and Paragraph 0043, encryption designed to support any encryption/decryption algorithm).

12. As per claim 8, Evoy discloses the reconfigurable logic device is an FPGA (Evoy, Paragraph 0066, FPGA used with access control functionality).

13. As per claim 11, Evoy discloses the processor, and a memory device in communication with the reconfigurable logic device, wherein the content of the memory device is accessible by the reconfigurable logic device but is not accessible by the processor, wherein the processor is configured to send a request for stored data, the request to be fulfilled at least in part by the reconfigurable logic device, and wherein the reconfigurable logic device is further configured to store at least a portion of the

decrypted data in the memory device (Evoy, Paragraph 0023, re-encrypts a digital data stream that has been decrypted).

14. As per claim 13, Evoy discloses wherein the data store comprises a hard disk drive system, the device further comprising a disk connector for interfacing the device with the hard disk drive system (Evoy, Paragraph 0037, hard disks).

15. As per claim 14, Evoy discloses a disk controller in communication with the disk connector and the reconfigurable logic device (Evoy, Paragraph 0037, hard disks).

16. As per claim 15, Evoy discloses an internal bus connecting the disk controller with the reconfigurable programmable logic device (Evoy, Paragraph 0033, PCI-Express communications).

17. As per claim 16, Evoy discloses the internal bus is a PCI-X bus(Evoy, Paragraph 0033, PCI-Express communications).

18. As per claim 17, Evoy discloses a bus connector for interfacing the reconfigurable logic device with a bus on a computer motherboard (Evoy, Paragraph 0033, PCI-Express communications).

19. As per claim 18, Evoy discloses wherein the bus connector is a PCI-X bus connector (Evoy, Paragraph 0033, PCI-Express communications).

20. As per claim 19, Evoy discloses the reconfigurable programmable logic device is an FPGA (Evoy, Paragraph 0066, FPGA used with access control functionality).

21. As per claim 21, Evoy discloses providing the authorized requester with a key for decrypting the delivered data (Evoy, Paragraph 0044, public key for decryption).

22. As per claim 45, Evoy discloses internal memory that is not accessible to the processor, and wherein the reconfigurable logic device is further configured to store the decrypted data only in its internal memory (Evoy, Paragraph 0056, circuitry coupled to a memory).

23. As per claim 46, Evoy discloses a processing board on which the reconfigurable logic device is deployed, the processing board in communication with the processor and the data store via a system bus, the processing board further comprising a memory device that is not accessible to the processor, wherein the reconfigurable logic device is further configured to store the decrypted data only in the memory device (Evoy, Paragraph 0038, circuitry, separate circuit boards).

24. As per claim 47, Evoy discloses a processing board on which the reconfigurable logic device is deployed, wherein the reconfigurable logic device includes internal memory that is not accessible to the processor, the processing board in communication with the processor and the data store via a system bus (Evoy, Paragraph 0056, circuitry coupled to a memory), the processing board further comprising a memory device that is not accessible to the processor, and wherein the reconfigurable logic device is further configured to store a portion of the decrypted data in its internal memory and store another portion of the decrypted data in the memory device (Evoy, Paragraph 0038, circuitry, separate circuit boards).

25. As per claims 51 and 63, Evoy discloses comprises a Field Programmable Gate Array (FPGA), wherein the network interface is configured to receive a request for data from the data store via a network, and wherein the processor is configured to request

that the FPGA initiate the data transfer in response to the request received by the network interface (Evoy, Paragraph 0066, FPGA used with access control functionality).

26. As per claims 52 and 64, Evoy discloses wherein the reconfigurable logic device comprises a programmable logic device (Evoy, Paragraph 0066, FPGA used with access control functionality).

27. As per claim 57, Evoy discloses wherein the reconfigurable logic device includes internal memory that is not accessible to the processor, the method further comprising: the reconfigurable logic device storing the decrypted data only in its internal memory (Evoy, Paragraph 0056, circuitry coupled to a memory).

28. As per claim 58, Evoy discloses the reconfigurable logic device is deployed on a processing board, the processing board in communication with the processor and the data store via a system bus, the processing board comprising a memory device that is not accessible to the processor, the method further comprising: the reconfigurable logic device storing the decrypted data only in the memory device (Evoy, Paragraph 0056, circuitry coupled to a memory).

29. As per claim 59, Evoy discloses the reconfigurable logic device storing a portion of the decrypted data in its internal memory and storing another portion of the decrypted data in the memory device (Evoy, Paragraph 0056, circuitry coupled to a memory).

***Claim Rejections - 35 USC § 103***

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy U.S. PG-Publication No. (2006/0059213) in view of Bankier et al. U.S. PG-Publication No. (2002/0103663).

32. As per claim 12, Evoy fails to teach wherein the reconfigurable logic device is also configured to perform a socket operation on incoming and outgoing data to interface the reconfigurable logic device with upstream and downstream components. However, in an analogous art Bankier teaches wherein the reconfigurable logic device is also configured to perform a socket operation on incoming and outgoing data to interface the reconfigurable logic device with upstream and downstream components (Bankier, Paragraph 0219, streamed data using SSL).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Bankier's Highly available transaction failure detection and recovery for electronic commerce transactions with Evoy's Dedicated encrypted virtual channel in a multi-channel serial communications interface because it offers the advantage of detecting failures in transactions (Bankier, Paragraph 0010).

33. Claims 48, 46 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy U.S. PG-Publication No. (2006/0059213) in view of Liu et al. U.S. PG-Publication No. (2003/0169877).

34. As per claims 48, 56 and 60, Evoy fails to teach a data processing pipeline, the pipeline comprising a decryption engine and a downstream encryption engine, wherein the reconfigurable logic device performs the decryption operation using the decryption engine and performs the encryption operation using the encryption engine. However, in an analogous art Liu teaches a data processing pipeline, the pipeline comprising a decryption engine and a downstream encryption engine, wherein the reconfigurable logic device performs the decryption operation using the decryption engine and performs the encryption operation using the encryption engine (Liu, Paragraph 0023, Pipelined decryption).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Liu's pipelined engine for encryption/authentication in IPSec with Evoy's Dedicated encrypted virtual channel in a multi-channel serial communications interface because it offers the advantage of improving efficiency of encryption (Liu, Paragraph 0012).

35. Claims 49, 50, 54, 55 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy U.S. PG-Publication No. (2006/0059213) in view of Okuda et al. U.S. PG-Publication No. (2004/0117645).

36. As per claim 49, Evoy fails to teach a search engine positioned between the decryption engine and the encryption engine, wherein the search engine is configured to search the decrypted data stream to find a targeted subset of the decrypted data in response to a data request, wherein the encryption engine is configured to perform the encryption operation by encrypting the targeted subset in the second encrypted format, and wherein the data for sharing comprises the targeted subset encrypted in the second encrypted format. Okuda teaches a search engine positioned between the decryption engine and the encryption engine, wherein the search engine is configured to search the decrypted data stream to find a targeted subset of the decrypted data in response to a data request, wherein the encryption engine is configured to perform the encryption operation by encrypting the targeted subset in the second encrypted format, and wherein the data for sharing comprises the targeted subset encrypted in the second encrypted format (Okuda, Paragraph 0023, stream analyzer).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Okuda's information reproducing apparatus with Evoy's dedicated encrypted virtual channel in a multi-channel serial communications interface because it offers the advantage of improving security copyright protection (Okuda, Paragraph 0021).

37. As per claims 50 and 62, Evoy as modified teaches a remote processor in communication with the reconfigurable logic device via a network and a network interface, and wherein reconfigurable logic device is further configured to receive the

data request from the remote processor (Evoy, Paragraph 0023, receive encrypted data and decrypt encrypted data).

38. As per claim 54, Evoy fails to teach the processor, wherein the processor is configured to communicate a search query request for the targeted data subset to the reconfigurable logic device, the search query request comprising a specification of a data key for use in the search operation. However, in an analogous art Okuda teaches the processor, wherein the processor is configured to communicate a search query request for the targeted data subset to the reconfigurable logic device, the search query request comprising a specification of a data key for use in the search operation (Okuda, Paragraph 0023, stream analyzer).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Okuda's information reproducing apparatus with Evoy's dedicated encrypted virtual channel in a multi-channel serial communications interface because it offers the advantage of improving security copyright protection (Okuda, Paragraph 0021).

39. As per claim 55, Evoy as modified teaches the device serves as an access gateway for communication with the data store, the access gateway comprising a network interface in communication with the reconfigurable logic device, the network interface configured to receive a search query request from the processor via a network and provide the received search query request to the reconfigurable logic device, the search query request comprising a specification of a data key for use in the search operation (Okuda, Paragraph 0023, stream analyzer).

40. Claims 61 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy U.S. PG-Publication No. (2006/0059213) in view of Liu et al. U.S. PG-Publication No. (2003/0169877) and Okuda et al. U.S. PG-Publication No. (2004/0117645).

41. As per claim 61, Evoy fails to teach the search engine searching the decrypted data stream to find a targeted subset of the decrypted data in response to a data request, wherein the encryption step comprises the encryption engine encrypting the targeted subset in the second encrypted format, and wherein the shared data comprises the targeted subset encrypted in the second encrypted format. However, in an analogous art Okuda teaches the search engine searching the decrypted data stream to find a targeted subset of the decrypted data in response to a data request, wherein the encryption step comprises the encryption engine encrypting the targeted subset in the second encrypted format, and wherein the shared data comprises the targeted subset encrypted in the second encrypted format (Okuda, Paragraph 0023, stream analyzer).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Okuda's information reproducing apparatus with Evoy's dedicated encrypted virtual channel in a multi-channel serial communications interface because it offers the advantage of improving security copyright protection (Okuda, Paragraph 0021).

42. As per claim 62, Evoy as modified teaches a remote processor in communication with the reconfigurable logic device via a network and a network interface, the method

further comprising the reconfigurable logic device receiving the data request from the remote processor (Evoy, Paragraph 0023, receive encrypted data and decrypt encrypted data).

## *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roderick Tolentino whose telephone number is (571) 272-2661. The examiner can normally be reached on Monday - Friday 9am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on (571) 272-3811. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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